compared to the number that could be stored if separate TLBs were used for GART and GTT entries." Specification at 9-10.

The Examiner contends that:

> As per claims 1 and 13, Fisher et al. substantially disclosed the invention as claimed, including a memory controller hub comprising: a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61) and available to an external graphics controller hub to store graphics data (Fig. 1, Item No. 18). Fisher et al did not explicitly disclose that the controller hub includes an internal graphics subsystem adapted to perform graphics operations on data. However, Ajanovic et al disclosed a memory controller which includes an internal graphics subsystem adapted to perform graphics operations on data (Fig. Items No. 110, 113; col 3, lines 45-47). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented the memory controller hub of Ajanovic et al into the system of Fisher et al because doing so would provide a more flexible and expandable graphics system by allowing the memory controller to accommodate a plurality of interfaces such as graphics interface and interface controller.
>
> As per claim 7, Fisher et al. substantially disclosed the invention as claimed, including a CPU (Fig. 1, Item No. 10); a display device (Fig. 1, Item No. 24); a system memory adapted to store video data and non-video data; and a memory controller hub coupled to the CPU (Fig. 1, Item No. 12) and coupled to the system memory (Fig. 1, Item No. 14), the memory controller hub comprising: a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61)and available to the memory controller hub to store graphics data (Fig. 1, Item No. 18).

Applicant disagrees, because Fisher does not disclose or suggest "[a] memory controller comprising a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and available to an external graphics controller coupled to the memory controller hub to store graphics data."

Fisher describes a memory controller hub (FIG. 1, Item No. 12). Fisher also mentions a "cache." Fisher mentions the cache exactly once, stating that "texture mapping hardware subsystems typically include a local memory cache that stores texture mapping data . . . ." Col. 1:58-60. However, Fisher does not disclose or suggest any connection between the memory controller hub and the cache, and there is simply no indication that the memory controller comprises a cache.

Applicant submits that when seeking to establish that a claim is obvious under 35 U.S.C. § 103, it is insufficient for the Office simply to cite a reference in which certain key words of the claim appear. Rather, the reference must "describe all of the elements of the claim, arranged as in the [claimed] device." C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349 (Fed. Cir. 1998). Here, the Examiner points to the portions of Fisher that describe a memory controller hub and that mention a cache, but the claim requires more than just a memory controller hub and a cache, and Fisher does not describe what the claim requires. Specifically, Fisher does not describe a memory controller that comprises a cache. Fisher itself does not provide any connection between the cache and the memory controller hub, and the Examiner does not explain why one or ordinary skill in the art would perceive a connection between the cache and the hub.

Indeed, Fisher suggests that graphics data are not stored in a cache within the local memory controller hub. For example, FIG. 1 shows a graphics controller (Item 18) that is external to the memory controller hub, and FIG. 2 shows that the graphics controller includes frame buffer memory (Item No. 56). The frame buffer memory within the graphics controller is used to store graphics data concerning rendered images, so that rasterization, scaling, and texturizing can be performed quickly on the images by the graphics engines within the graphics controller. See col. 4:30-55. Because the graphics controller contains its own frame buffer memory, an additional cache located within the memory controller and outside the graphics controller would seem superfluous and unnecessary. Thus, Fisher suggests that the memory controller hub does not comprise a cache.

In addition, Fisher does not disclose or suggest a cache within a memory controller hub that is adapted to store addresses of locations in physical memory available to an internal graphics subsystem for storing graphics data. The Examiner asserts baldly that the cache in Fisher is "adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61) and [is] available to an external graphics controller hub to store graphics data (Fig. 1, Item No. 18)." Office action at page 2. However, the portions of Fisher cited by the Examiner do not provide any support for the Examiner's contention that the cache is adapted to store addresses of locations in physical memory or that the

cache is available to an external graphics controller to store graphics data. If the Examiner maintains his contention, applicant respectfully requests that the Examiner provide support within Fisher for his assertion that the cache is particularly adapted as claimed.

Ajanovic does not remedy the deficiencies of Fisher. Ajanovic does not disclose or suggest a memory controller hub comprising a cache, nor does Ajanovic disclose or suggest "a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and available to an external graphics controller coupled to the memory controller hub to store graphics data."

Additionally, applicant disagrees with the Examiner's contention that "Ajanovic et al. disclosed a memory controller which includes an internal graphics subsystem adapted to perform graphics operations on data (Fig. Items No. 110, 113, col. 3, lines 45-47)." In fact, Ajanovic discloses a memory controller hub 110 that includes a graphics interface 113 (col. 3:45-53 and Fig. 1). However, the graphics interface 113 is not adapted to perform graphics operations on data. Rather, graphics interface 113 is coupled to a graphics accelerator 130 and is used to export data from the memory controller hub 110 to the graphics accelerator 130, where the graphics accelerator performs graphics operations on the data. Thus, Ajonovic's memory controller hub does not include an internal graphics subsystem adapted to perform graphics operations on data.

Independent claims 1, 7, and 13 are allowable for at least the foregoing reasons. Claims 2-6 depend from claim 1 and are allowable at least for the same reasons that the claims 1 is allowable. Claims 8-12 depend from claim 7 and are allowable at least for the same reasons that the claims 7 is allowable. Claims 14-16 depend from claim 13 and are allowable at least for the same reasons that the claims 13 is allowable.

Enclosed is a $420 check for the Petition for Extension of Time fee. A two-month fee is being paid at this time because applicant replied to the June 11, 2003, final Office action on August 11, 2003, but the Office did not mail an advisory action until October 22, 2003. See MPEP 706.07. Please apply any other charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-165001.

Respectfully submitted,

Date: 12/10/03

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